**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (Currently Amended) A managing system for managing a plurality of VRMs associated with a plurality of microprocessors and connected in parallel together between first and second supply voltage references, said VRMs having output terminals connected together and arranged to communicate over a common bus receiving an output current signal from said plurality of VRMs, wherein said managing system comprises:

an equivalent droop resistor;

an error amplifier receiving input signals, said~~being~~ input signals including an output voltage signal from said plurality of VRMs, a reference voltage (Vref), and a droop voltage produced through the~~an~~ equivalent droop resistor ~~receiving an output current signal (Iout) from said plurality of VRMs and being connected to said common bus~~, said error amplifier effecting a comparison of said input signals to generate a control voltage signal to said plurality of VRMs; ~~and~~

first and second control resistors connected, in series with each other, to said common bus to receive said output current signal;

a third summing node, being input a first local control voltage from said first control resistor as a positive addend and a second local control voltage from said second control resistor as a negative addend; and

a controller connected to an output of said third summing node and said equivalent droop resistor for supplying an internal control current to said equivalent droop resistor.

2. (Currently Amended) A managing system according to claim 1, comprising:

at least a first summing node, being connected to said error amplifier and said equivalent droop resistor ~~and arranged to output a control voltage signal to said plurality of VRMs~~, said first summing node receiving the~~a~~ reference voltage as a positive addend and receiving, as negative addends, the~~a~~ droop voltage and a total voltage resulting from a summation, performed in a second summing node, of the~~an~~ output voltage signal from said plurality of VRMs~~,~~ and said second supply voltage reference~~;~~

~~first and second control resistors connected, in series with each other, to said common bus to receive said output current signal; and~~

~~a third summing node, being input a first local control voltage from said first control resistor as a positive addend and a second local control voltage from said second control resistor as a negative addend;~~

~~wherein said controller is connected to an input of said third summing node and supplies an internal control voltage directly to said equivalent droop resistor~~.

3. (Currently Amended) A managing system according to Claim 2, wherein said error amplifier comprises an operational amplifier having a first input terminal to receive said reference voltage and an output terminal feedback-connected, through a capacitor, to a second input terminal thereof, said second input terminal being connected to an internal circuit node, said internal circuit node receiving the sum of a droop current (Idroop), the~~an~~ internal control current, and said output voltage signal from the VRM plurality through a feedback resistor (Rfb) passing said sum of currents.

4. (Currently Amended) A managing system according to Claim 3, further comprising

a compensation resistor (Rc) connected to said internal circuit node; and

an amplifier that supplies to the~~wherein said internal circuit node is connected to a compensating sub-system, said compensating sub-system comprising a~~ compensation resistor a ~~to receive the~~ sum of said control voltage and said reference voltage.

5. (Currently Amended) A managing system according to Claim 4, wherein a regulated voltage signal is output being equal to:

Vref – Idroop*Rfb – Vshare*Rfb/Rc,

said droop current being proportional to the value of said output current signal from the VRM plurality, and said control voltage (Vshare) being proportional to the ratio Iload/N-Iout, where N is the number of cascaded modules in said VRM plurality.

6-12. (Canceled)

13. (Currently Amended) A control system for controlling a first voltage reference module that outputs an output voltage, comprising:

a first error amplifier having a first input and an output, the first input being coupled to the output;

~~a feedback resistor coupled between the output voltage and the first input of the first error amplifier;~~

a first current generator coupled to the first input of the first error amplifier; ~~and~~

a controller having a second current generator coupled to the first input of the first error amplifier, the second current generator being responsive to a voltage on a common bus connected between the first voltage reference module and a second voltage reference module;

a second error amplifier having a first input coupled to the common bus, a second input coupled to the first input of the first error amplifier, and an output coupled to the second current generator;

a share resistor coupled between the common bus and the second input of the second error amplifier;

a first resistor connected between the share resistor and the first input of the second error amplifier; and

a second resistor connected between the share resistor and the second input of the second error amplifier, the first resistor, share resistor, and second resistor being connected in series with each other.

14. (Original) A control system according to claim 13 wherein the first error amplifier further comprises a second input coupled to a voltage reference.

15-18. (Canceled)

19. (Currently Amended) A control system for controlling a first voltage reference module that outputs an output voltage, comprising:

a first error amplifier having first and second inputs and an output;

a feedback resistor coupled between the output voltage and the first input of the first error amplifier; ~~and~~

a second error amplifier having a first input coupled to a common bus, a second input coupled to one of the inputs of the first error amplifier, and an output coupled to the first input of the first error amplifier, the common bus being connected to the first voltage reference module and a second voltage reference module;

a share resistor coupled between the common bus and the second input of the second error amplifier;

a first resistor connected between the share resistor and the first input of the second error amplifier; and

a second resistor connected between the share resistor and the second input of the second error amplifier, the first resistor, share resistor, and second resistor being connected in series with each other.

20. (Previously Presented) A control system according to claim 19, further comprising a first current generator coupled between the output of the second error amplifier and the first input of the first error amplifier.

21. (Previously Presented) A control system according to claim 20, further comprising a second current generator coupled to the first input of the first error amplifier.

22. (Previously Presented) A control system according to claim 19 wherein the first error amplifier further comprises a second input coupled to a voltage reference.

23-24. (Canceled)

25. (Previously Presented) A control system according to claim 13 wherein the output and first input of the first error amplifier are feedback-connected to one another.